CMOS Digital Integrated Circuits

Chapter 1
Introduction

S.M. Kang and Y. Leblebici
Some History

Invention of the transistor (BJT) 1947
Shockley, Bardeen, Brattain – Bell Labs

Single-transistor integrated circuit 1958
Jack Kilby – Texas Instruments

Invention of CMOS logic gates 1963
Wanlass & Sah – Fairchild Semiconductor

First microprocessor (Intel 4004) 1970
2,300 MOS transistors, 740 kHz clock frequency

Very Large Scale Integration 1978
Chips with more than ~20,000 devices
More Recently

**Ultra Large Scale Integration**

**System on Chip (SoC)**

20 ~ 30 million transistors in 2002

The chip complexity has increased by a factor of 1000 since its first introduction, but the term **VLSI** remained virtually universal to denote digital integrated systems with high complexity.
As a result of the continuously increasing integration density and decreasing unit costs, the semiconductor industry has been one of the fastest growing sectors in the worldwide economy.
Industry Trends

Large
Centralized
Expensive

Small / Portable
Distributed
Inexpensive
Industry Trends

High performance
Low power dissipation
Wireless capability
etc…

More portable, wearable, and more powerful devices for ubiquitous and pervasive computing…
Some Leading-Edge Examples

Intel Pentium 4
0.13μ process
55 million transistors
2.4GHz clock
145mm²
Some Leading-Edge Examples

IBM S/390 Microprocessor
0.13 μm CMOS process
7 layers Cu interconnect
47 million transistors
1 GHz clock
180 mm²
Evolution of Minimum Feature Size

![Graph showing the evolution of minimum feature size from 1975 to 2000. The feature size decreases significantly over time, from approximately 4.0 µm in 1975 to 0.1 µm in 2000. The graph includes data points for each year, indicating a steady decrease in feature size.](image.png)
Evolution of Minimum Feature Size

2002: 130 nm
2003: 90 nm
...
2010: 35 nm (?)
Moore’s Law

- Memory (rate of increase = x 1.5 / year)
- Microprocessor (rate of increase = x 1.25 / year)

Source: Intel Corp.
Evolution of Memory Capacity
### ITRS - International Technology Roadmap for Semiconductors

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Predictions of the worldwide semiconductor / IC industry about its own future prospects...
# Shrinking Device Dimensions

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Increasing Function Density

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### Increasing Clock Frequency

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5-layer cross-section of chip
Typical Chip Cross Section

- Passivation
- Dielectric
- Etch stop layer
- Dielectric diffusion barrier
- Copper conductor with metal barrier liner
- Pre-metal dielectric
- Tungsten contact plug
System-on-Chip

Integrating all or most of the components of a hybrid system on a single substrate (silicon or MCM), rather than building a conventional printed circuit board.

1. More compact system realization

2. Higher speed / performance
   - Better reliability
   - Less expensive!
New Direction: System-on-Chip (SoC)
Products have a shorter life-cycle!

![Diagram showing product revenue over product lifecycle (months)]
longer design time for better performance in current generation

missed technology window = lower performance in next generation
Better strategy
The Y-Chart

Notice: There is a need for structured design methodologies to handle the high level of complexity!
Simplified VLSI Design Flow

Top-down

Bottom-up
Structured Design Principles

Hierarchy: “Divide and conquer” technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.

Regularity: The hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

Modularity: The various functional blocks which make up the larger system must have well-defined functions and interfaces.

Locality: Internal details remain at the local level. The concept of locality also ensures that connections are mostly between neighboring modules, avoiding long-distance connections as much as possible.
Hierarchy of a 4-bit Carry Ripple Adder
Hierarchy of a 16-bit Manchester Adder

- 16 bit adder
- 4 bit adder with Manchester carry
  - Manchester carry circuit block
- 4 bit adder with Manchester carry
  - carry - propagate circuit block
- 4 bit adder with Manchester carry
  - output buffer
- 4 bit adder with Manchester carry
  - XOR gate
Hierarchy of a 16-bit Manchester Adder
Hierarchy of a 16-bit Manchester Adder

4-bit adder with Manchester carry
Hierarchy of a 16-bit Manchester Adder

- Carry/propagate circuit layout
- Manchester carry circuit layout
- Output buffer/latch circuit layout
Regularity

2-input MUX

DFF
Full Custom Design

Following the partitioning, the transistor level design of the building block is generated and simulated.

The example shows a 1-bit full-adder schematic and its SPICE simulation results.
Full Custom Design

The main objective of full custom design is to ensure fine-grained regularity and modularity.
A carefully crafted full custom block can be placed both along the X and Y axis to form an interconnected two-dimensional array.

Example:

Data-path cells
Full Custom SRAM Cell Design
Mapping the Design into Layout

Manual full-custom design can be very challenging and time consuming, especially if the low level regularity is not well defined!
HDL-Based Design

1980’s
Hardware Description Languages (HDL) were conceived to facilitate the information exchange between design groups.

1990’s
The increasing computation power led to the introduction of logic synthesizers that can translate the description in HDL into a synthesized gate-level net-list of the design.

2000’s
Modern synthesis algorithms can optimize a digital design and explore different alternatives to identify the design that best meets the requirements.
The design is synthesized and mapped into the target technology.

The logic gates have one-to-one equivalents as standard cells in the target technology.
Standard Cells

AND  DFF  INV  XOR
Standard Cells
Standard Cells
Standard Cells

Rows of standard cells with routing channels between them

Memory array
Standard Cells
VLSI Design Styles

- Full-custom
- Semi-custom
  - Masked gate array (MGA)
  - Cell-based (CBIC) (standard cells)
- Programmable
  - PLD
  - CPLD
  - FPGA
Mask Gate Array

two-step manufacture:

first (deep) processing steps

standard masks

base wafers

customization: contacts & metal layers

custom masks

ASIC
Mask Gate Array

Before customization
VLSI Design Styles

- Full-custom
- Semi-custom
- Programmable
  - Masked gate array (MGA)
  - Cell-based (CBIC) (standard cells)
  - PLD
  - CPLD
  - FPGA
Field Programmable Gate Array
Field Programmable Gate Array

Internal structure of a CLB
Field Programmable Gate Array

Six Pass Transistors
Per Switch Matrix
Interconnect Point

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