Categories of Materials

Materials can be categorized into three main groups regarding their electrical conduction properties:

- **Insulators**
- **Conductors**
- **Semiconductors**
Semiconductors

While there are numerous semiconductor materials available, by far the most popular material is Silicon.

GaAs, InP and SiGe are compound semiconductors that are used in specialized devices.

The success of a semiconductor material depends on how easy it is to process and how well it allows reliable high-volume fabrication.
Single Crystal Growth

Pure silicon is melted in a pot (1400°C) and a small seed containing the desired crystal orientation is inserted into molten silicon and slowly (1mm/minute) pulled out.
Single Crystal Growth

The silicon crystal (in some cases also containing doping) is manufactured (pulled) as a cylinder with a diameter of 8-12 inches.

This cylinder is carefully sawed into thin disks (wafers). The wafers are later polished and marked for crystal orientation.
An IC consists of several layers of material that are manufactured in successive steps.

**Lithography** is used to selectively process the layers, where the 2-D mask geometry is copied on the surface.
Lithography

The surface of the wafer is coated with a photosensitive material, the **photoresist**. The mask pattern is developed on the photoresist, with UV light exposure.

Depending on the type of the photoresist (negative or positive), the exposed or unexposed parts of the photoresist change their property and become resistant to certain types of solvents.

Subsequent processing steps remove the undeveloped photoresist from the wafer. The developed pattern (usually) protects the underlying layer from an etching process. The photoresist is removed after patterning on the lower layer is completed.
Etching

Etching is a common process to pattern material on the surface. Once the desired shape is patterned with photoresist, the unprotected areas are etched away, using wet or dry etch techniques.
Patterning of Features on SiO$_2$
Patterning of Features on SiO$_2$
Oxide Growth / Oxide Deposition

Oxidation of the silicon surface creates a SiO$_2$ layer that acts as an insulator. Oxide layers are also used to isolate metal interconnections.

An annealing step is required to restore the crystal structure after thermal oxidation.
**Ion Implantation**

Ion implantation is used to add doping materials to change the electrical characteristics of silicon locally. The dopant ions penetrate the surface, with a penetration depth that is proportional to their kinetic energy.
While some of the structures can be grown on silicon substrate, most of the other materials (especially metal and oxide) need to be deposited on the surface.

In most cases, the material that is deposited on the whole surface will be patterned and selectively etched.

There are two main methods for thin film deposition:

- PVD  Physical Vapor Deposition
- CVD Chemical Vapor Deposition
Fabrication of an nMOS Transistor

(a) Si - substrate

(b) SiO₂ (Oxide)

(c) SiO₂ (Oxide)

(d) Thin oxide
    SiO₂ (Oxide)
    Si - substrate
Fabrication of an nMOS Transistor
Fabrication of an nMOS Transistor

(h) Polysilicon

(i) Insulating oxide

(j) Insulating oxide
Fabrication of an nMOS Transistor
CMOS Process

The CMOS process allows fabrication of nMOS and pMOS transistors side-by-side on the same Silicon substrate.
CMOS Process Flow

1. Create n-well regions and channel-stop regions
2. Grow field oxide and gate oxide (thin oxide)
3. Deposit and pattern polysilicon layer
4. Implant source and drain regions, substrate contacts
5. Create contact windows, deposit and pattern metal layer
The first step of processing is to create a deeply implanted n-well.

This is done either by diffusion or ion implantation.
Definition of Active Areas

The next step is to define the active areas where the transistors will later be created.

A thermal oxide is grown uniformly on the surface. Then the active areas are covered by nitride. A second thermal oxidation process grows thick silicon dioxide outside the active areas.
Polysilicon Deposition

The entire surface is covered with a thin oxide layer (gate oxide).

Polysilicon is deposited and patterned to form the gates of the nMOS and pMOS transistors.
Source/Drain Implantation

The drain and source regions of the nMOS and pMOS transistors are created by doping.
Oxide Deposition

The entire surface is covered with a field oxide and the contact holes are etched into this oxide to enable connection to the underlying layers.
The metal layer is deposited using a Physical Vapor Deposition (PVD) method, patterned, and etched.
The entire surface is covered with a field oxide and the contact holes are etched into this oxide to enable connection to the underlying layers.

Then, the second (third, fourth, etc…) layer of metal can be deposited, patterned and etched according to the mask layout.
Lithography Masks

- Each lithography step during fabrication must be defined by a separate lithography mask.
- Each mask layer is drawn (either manually or using a design automation tool) according to the layout design rules.
- The combination (superposition) of all necessary mask layers completely defines the circuit to be fabricated.
active
poly
implant
contacts
metal
Composite Mask Layout

GND  n-type diffusion  Output  p-type diffusion  VDD

Input

n-well

nMOS  pMOS
Layout Design Rules

- To allow reliable fabrication of each structure, the mask layers must conform to a set of geometric layout design rules.

- Usually, the rules (for example: minimum distance and/or separation between layers) are expressed as multiples of a scaling factor – lambda (\( \lambda \)).

- For each different fabrication technology, lambda factor can be different.
Layout Design Rules
Layout Design Rules

Contact
5.1 Exact contact size 2λ
5.2 Min. poly overlap 1.5λ
5.3 Min. spacing 2λ
5.4 Min. spacing to gate 2λ
6.1 Exact contact size 2λ
6.2 Min. active overlap 1.5λ
6.3 Min. spacing 2λ
6.4 Min. spacing to gate 2λ

Metal 1
7.1 Min. width 3λ
7.2.a Min. spacing 3λ
7.3 Min. overlap of any contact 1λ

Via 1
8.1 Exact size 2λ
8.2 Min. spacing 3λ
8.3 Min. overlap by metal 1 1λ
8.4 Min. spacing to contact 2λ
8.5 Min. spac. to poly or act. edge 2λ

Metal 2
9.1 Min. width 3λ
9.2.a Min. spacing 4λ
9.3 Min. overlap to via 1 1λ

(*) Not Drawn
Layout Rules of a Minimum-Size MOSFET
minimum overlap of n-well over p+ active area

minimum separation between n+ active area and n-well

minimum separation between the nMOS and the pMOS transistor
State-of-the-Art Examples

Source: Nikkei Microdevices 9/02

(a) 90nm ノード向けトランジスタ
Multi-Level Interconnect with CMP
Multi-Level Metal Interconnect

TSMC
0.13μm
8 layers
Cu

Source:
Nikkei
Microdevices
11/00
Multi-Level Metal Interconnect

Source: Nikkei Microdevices 9/02

(b) 90nm ノード向け多層配線
Multi-Level Metal Interconnect
Silicon on Insulator (SOI)

The key innovation in SOI is to build the transistor structures on an **insulating** material rather than a common substrate as in CMOS. This reduces parasitic capacitances and eliminates substrate noise coupling.
Lithography Resolution is Decreasing

With each new technology generation, we would be able to fit the same amount of functionality into a **smaller** silicon area (ideally).
Lithography Resolution is Decreasing

But at the same time, we try to put more functionality in each chip for each new technology generation, so that the average chip size actually increases over the years!
Final Remark: Fabrication Cost

Initial investment costs of a new fabrication facility